

# Alaska® P Gen6 8L PCIe Retimer

Low-power, low-latency, 8-lane PCIe Gen 6/CXL 3 protocol-aware retimer  
P/N MV-CHP10080

## Overview

The Alaska® P Gen6 8L PCIe Retimer (MV-CHP10080) is an 8-lane, low-power, low-latency, fully PCI Express® Gen 6.x-compliant devices with leading I/O performance. It is capable of driving eight lanes of maximum 64 Gbps signal, extending the reach between PCIe root complex (RC) and end point (EP).

The MV-CHP10080 is optimized for low-latency applications with Compute Express Link™ 3.x protocol and its long-range SerDes on both sides (upstream and downstream) support signal transmission over high-loss channels.

The MV-CHP10080 can operate at 64 GT/s, 32 GT/s, 16 GT/s, 8 GT/s, 5 GT/s, and 2.5 GT/s PCIe Data Rate with automatic link equalization and training per PCIe specifications.

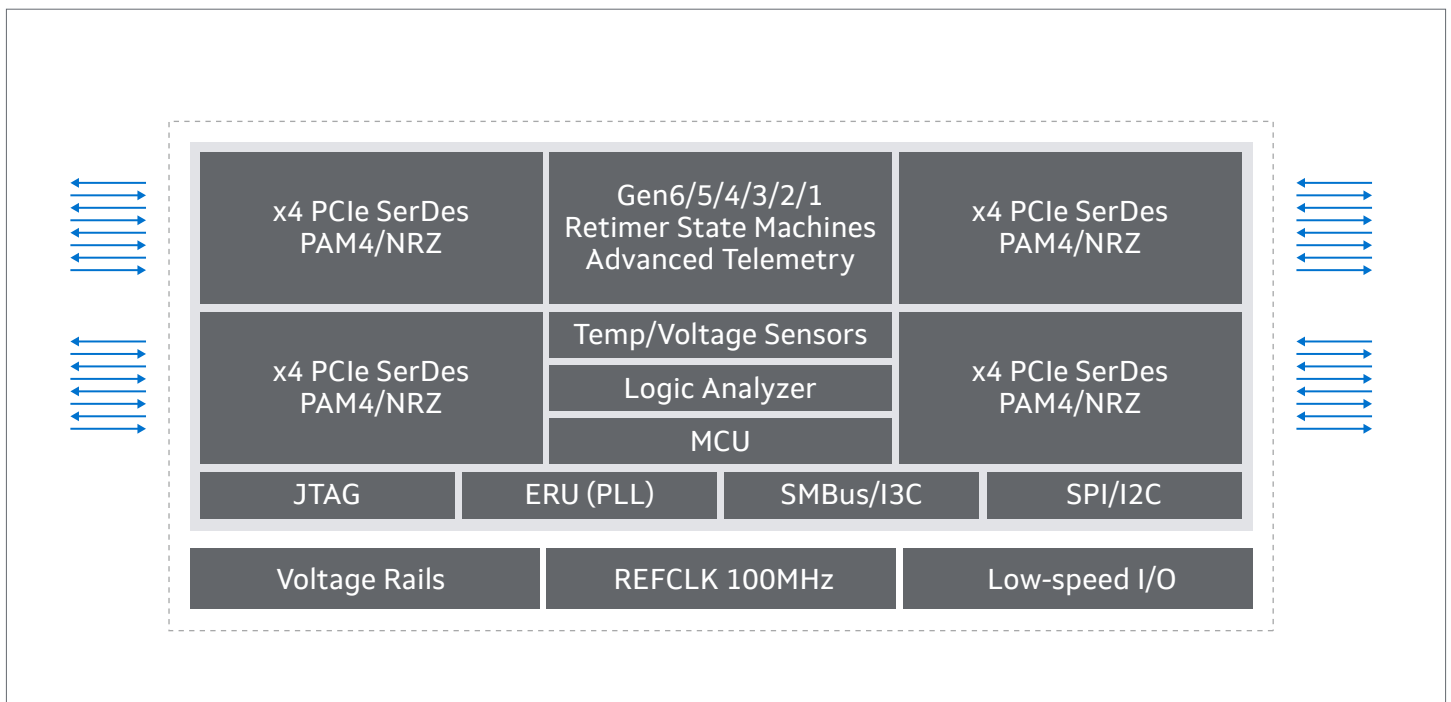
The MV-CHP10080 exceeds PCI-SIG electrical specifications with >32 dB Insertion Loss (IL) at 64 GT/s (PCIe 6) and >36 dB IL at 32 GT/s (PCIe 5). The device enables customers to scale compute fabric inside accelerated systems, general-purpose servers, and cache-coherent disaggregated infrastructure.

The MV-CHP10080 follows Intel PCIe 6.0 Retimer Supplemental Footprint and enables gen-to-gen design compatibility. The device is developed under advanced process node and provides significant power efficiency.

The MV-CHP10080 supports flexible link bifurcation, with one x8, two x4, four x2 and more combinations. The device takes PCIe base specification-compliant 100 MHz clock input and provides reference clock output to downstream devices. Common clock, SRIS, and SRNS are all supported clocking systems.

The MV-CHP10080 features advanced in-band and out-of-band diagnostics and telemetry functionality, supporting large-scale fleet management. It can be configured through SMBus/I3C or EEPROM/SPI flash for ease of adoption.

## Block Diagram



## Key Features

Features	Benefits
Standard and compatibility	<ul style="list-style-type: none"><li>• Compliant with PCI-SIG specifications for PCI Express® Gen-6.x/5/4/3/2/1</li><li>• Compliant with Compute Express Link™ 3.x/2.0/1.1</li><li>• Support cache-coherent application with low-latency mode</li><li>• 16 bi-directional PCIe lanes; 8-lane upstream and 8-lane downstream</li><li>• All lanes can operate at 64 GT/s, 32 GT/s, 16 GT/s, 8 GT/s, 5 GT/s, and 2.5 GT/s data rates</li><li>• Flexible link bifurcation from 1 x8, 2 x4, and up to 4 x2 lanes per link</li><li>• PCIe hot-add and hot-removal of end point devices independently on each link or partition</li></ul>
I/O performance	<ul style="list-style-type: none"><li>• First Bit Error Rate (FBER) better than 1E-6</li><li>• Support channel IL budget of &gt;32 dB for PCIe 6, &gt;36 dB for PCIe 5 at 16 GHz Nyquist frequency</li><li>• Advanced equalization features support various channel topologies</li></ul>
Clocking	<ul style="list-style-type: none"><li>• Support Common Clock, SRIS, and SRNS</li><li>• PCIe base specification compliant 100 MHz clock input</li><li>• HCSL reference clock output to downstream devices</li></ul>
Management	<ul style="list-style-type: none"><li>• I2C/SMBus-compatible management interface with additional I3C features</li><li>• On-chip voltage and thermal sensors</li></ul>
Design information	<ul style="list-style-type: none"><li>• Three external power rails</li><li>• Package options for integrated DC-blocking capacitors</li><li>• IBIS-AMI model for simulation</li><li>• Device configuration through SMBus/I3C, EEPROM or SPI Flash</li><li>• GPIO for quick indications of link status and functional status</li></ul>
Debug and diagnostics	<ul style="list-style-type: none"><li>• Advanced in-band and out-of-band diagnostics and telemetry features</li><li>• IEEE 1149.6 AC-JTAG boundary scan</li><li>• Embedded logic analyzer and history FIFO</li></ul>
Package characteristics	<ul style="list-style-type: none"><li>• MV-CHP10080: 8.9 mm×13.2 mm HFETBGA package with minimum 0.5 mm ball pitch</li></ul>

## Target Applications

- Motherboard PCIe/CXL trace-length extension
- Compute fabric of GPU/AI system
- PCIe riser card and backplane
- NVMe SSD storage and CXL disaggregated memory
- PCIe active electrical cable (PCIe AEC)



To deliver the data infrastructure technology that connects the world, we're building solutions on the most powerful foundation: our partnerships with our customers. Trusted by the world's leading technology companies over 25 years, we move, store, process and secure the world's data with semiconductor solutions designed for our customers' current needs and future ambitions. Through a process of deep collaboration and transparency, we're ultimately changing the way tomorrow's enterprise, cloud, automotive, and carrier architectures transform—for the better.

Copyright © 2024 Marvell. All rights reserved. Marvell and the Marvell logo are trademarks of Marvell or its affiliates. Please visit [www.marvell.com](http://www.marvell.com) for a complete list of Marvell trademarks. Other names and brands may be claimed as the property of others.

Marvell\_Alaska\_P MV-CHP10080\_PB Revised: 05/24