Marvell® Alaska® 88E1112

Integrated 10/100/1000 Gigabit Ethernet Transceiver

Technical Product Brief - Public

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Overview

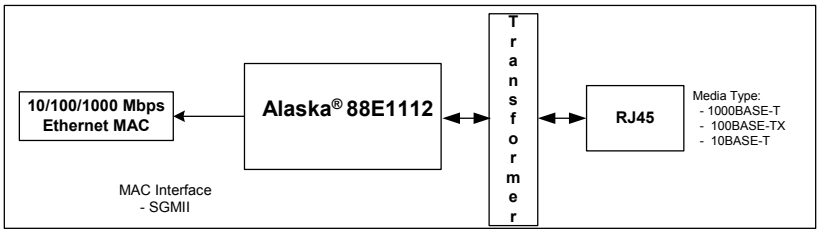
The Alaska® 88E1112 Gigabit Ethernet Transceiver is a physical layer device for Ethernet 1000BASE-T, 100BASE-TX, and 10BASE-T applications. It is manufactured using standard digital CMOS process and contains all the active circuitry required to implement the physical layer functions to transmit and receive data on standard CAT 5 unshielded twisted pair.

The Alaska 88E1112 device supports the Serial Gigabit Media Independent Interface (SGMII) for direct connection to a MAC/Switch port. The 88E1112 device incorporates an additional 1.25 GHz SERDES (Serializer/Deserializer) which may be connected directly to a fiber-optic transceiver for 1000BASE-X applications. The SERDES is switchable to support 125 MHz operation for 100BASE-FX applications. Additionally, the 88E1112 device may be used to implement 10/100/1000BASE-T Gigabit Interface Converter (GBIC) or Small Form Factor Pluggable (SFP) modules.

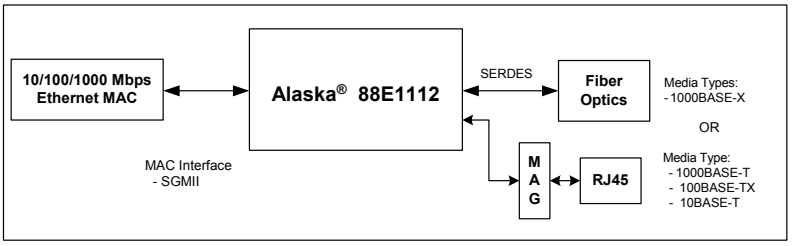
The 88E1112 device uses advanced mixed-signal processing to perform equalization, echo and crosstalk cancellation, data recovery, and error correction at a gigabit per second data rate. The device achieves robust performance in noisy environments with very low power dissipation.

Features

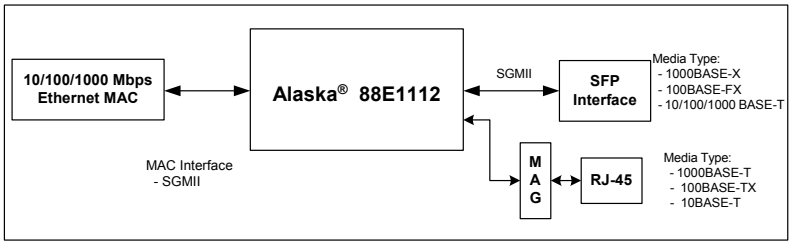
- 10/100/1000BASE-T IEEE 802.3 compliant
- Supports Serial Gigabit Media Independent Interface (SGMII)
- Integrated 1.25 GHz SERDES for 1000BASE-X fiber applications
- Integrated 125 MHz SERDES for 100BASE-FX fiber applications
- SGMII to SERDES mode supported
- SGMII to SGMII bridging supported
- Supports tri-speed GBIC/SFP applications
- Media Detection™ mode for copper and fiber support
- Integrated Virtual Cable Tester® (VCT™) cable diagnostic feature
- 2-pair downshift feature
- Auto-MDI/MDIX feature when link partner Auto-Negotiation enabled or disabled
- Advanced diagnostics: CRC error checker, packet counter, pattern generator
- EEPROM support for PHY configuration
- Selectable MDC/MDIO interface or Two-Wire Serial Interface
- Fully integrated digital adaptive equalizers, echo cancellers, and crosstalk cancellers
- Advanced digital baseline wander correction
- Automatic polarity correction
- IEEE 802.3u compliant Auto-Negotiation
- Requires only two supplies: 2.5V and 1.2V
- Very low power dissipation P_{AVE} = 0.75W
- Manufactured in a 64-Pin QFN, 9X9 mm package
- Available in Commercial or Industrial grade



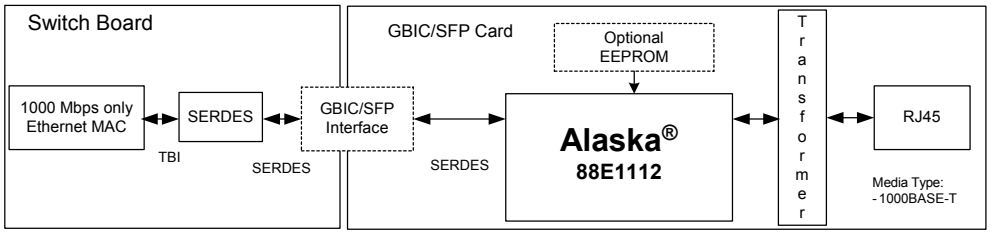
Alaska 88E1112 used in Copper Applications



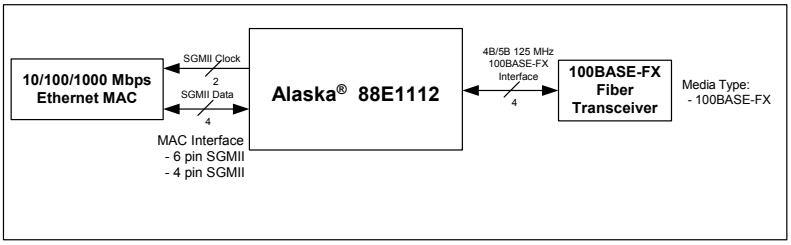
Alaska 88E1112 used in Media Detect™ Applications (1000BASE-X SERDES)



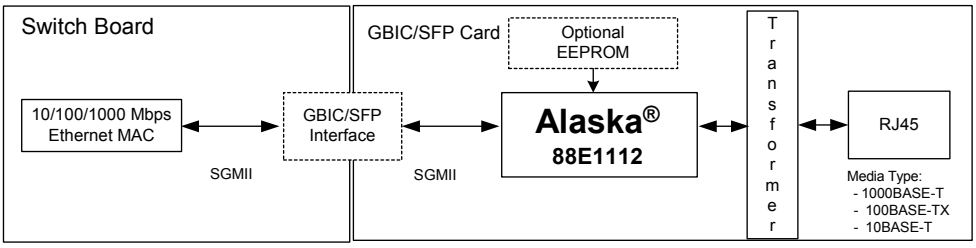
Alaska 88E1112 used in Media Detect ™ Applications (SGMII)



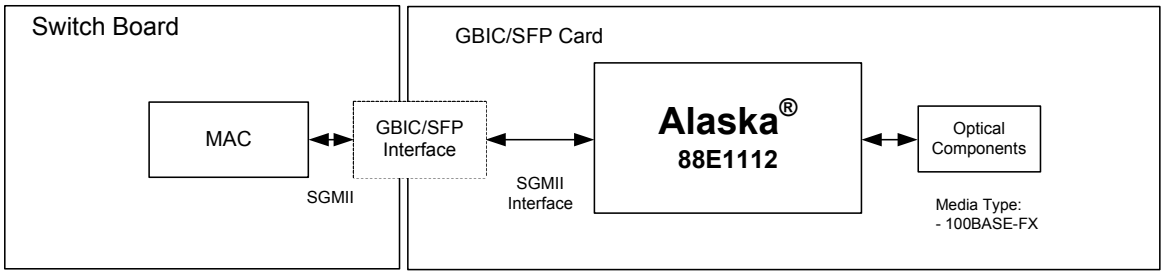
Alaska 88E1112 used in 1000BASE-T GBIC/ SFP Applications



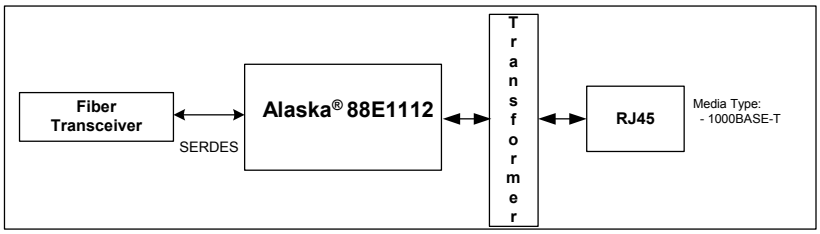
Alaska 88E1112 used in Traditional 100BASE-FX Applications



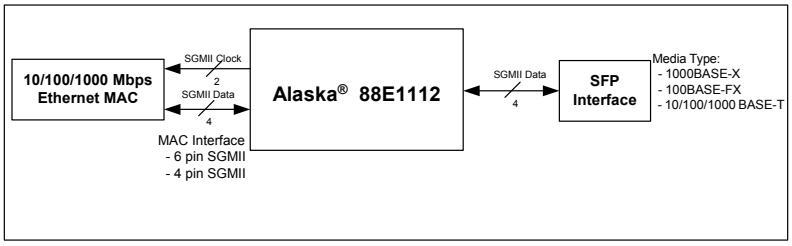
Alaska 88E1112 used in 10/100/1000BASE-T tri-speed GBIC/SFP Applications



Alaska 88E1112 used in 100BASE-FX GBIC/SFP Applications



Alaska 88E1112 used in Media Converter Applications



Alaska 88E1112 used in 4-pin SGMII to 6-pin SGMII Conversions

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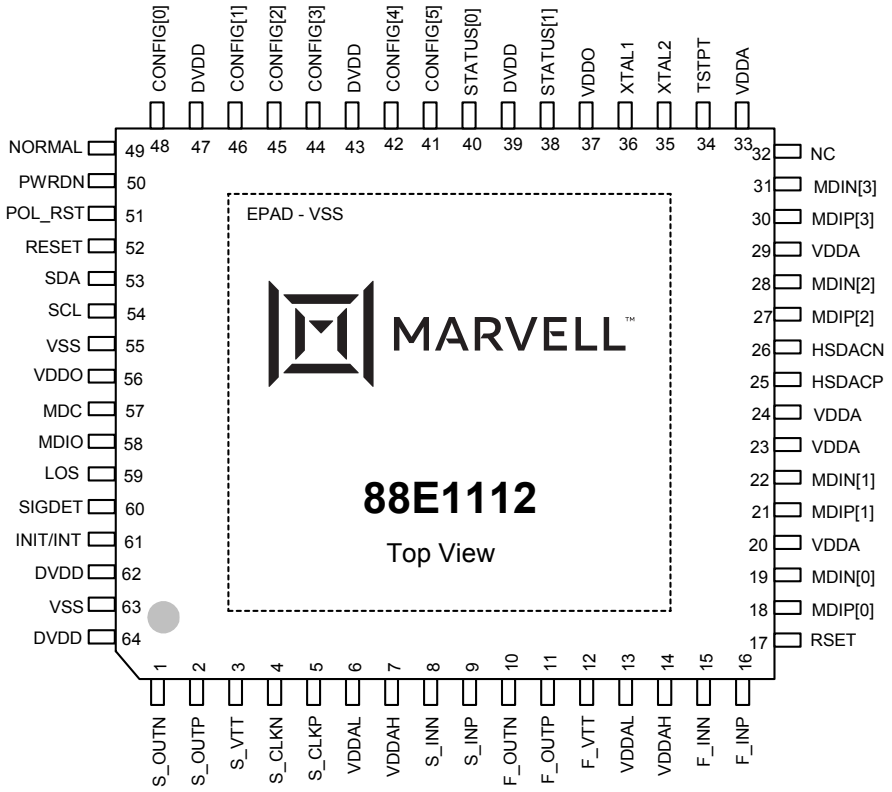
Section 1. Signal Description

The 88E1112 device is a 10/100/1000BASE-T/1000BASE-X/100BASE-FX Gigabit Ethernet transceiver.

1.1 88E1112 64-Pin QFN Package

Figure 1: 88E1112 64-Pin QFN Package (Top View)



1.2 Pin Description

1.2.1 Pin Type Definitions

Pin Type	Definition
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open drain output
Z	Tri-state output
mA	DC sink capability

Table 1: Copper Interface

Pin #	Pin Name	Pin Type	Description
18 19	MDIP[0] MDIN[0]	I/O	Media Dependent Interface[0]. In 1000BASE-T mode in MDI configuration, MDIP/N[0] correspond to BI_DA±. In MDIX configuration, MDIP/N[0] correspond to BI_DB±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIP/N[0] are used for the transmit pair. In MDIX configuration, MDIP/N[0] are used for the receive pair. MDIP/N[0] should be tied to ground if not used.
21 22	MDIP[1] MDIN[1]	I/O	Media Dependent Interface[1]. In 1000BASE-T mode in MDI configuration, MDIP/N[1] correspond to BI_DB±. In MDIX configuration, MDIP/N[1] correspond to BI_DA±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIP/N[1] are used for the receive pair. In MDIX configuration, MDIP/N[1] are used for the transmit pair. MDIP/N[1] should be tied to ground if not used.
27 28	MDIP[2] MDIN[2]	I/O	Media Dependent Interface[2]. In 1000BASE-T mode in MDI configuration, MDIP/N[2] correspond to BI_DC±. In MDIX configuration, MDIP/N[2] correspond to BI_DD±. In 100BASE-TX and 10BASE-T modes, MDIP/N[2] are not used. MDIP/N[2] should be tied to ground if not used.
30 31	MDIP[3] MDIN[3]	I/O	Media Dependent Interface[3]. In 1000BASE-T mode in MDI configuration, MDIP/N[3] correspond to BI_DD±. In MDIX configuration, MDIP/N[3] correspond to BI_DC±. In 100BASE-TX and 10BASE-T modes, MDIP/N[3] are not used. MDIP/N[3] should be tied to ground if not used.

Table 2: Fiber Interface: 1000BASE-X/SGMII Media Interface/100BASE-FX

Pin #	Pin Name	Pin Type	Description
16 15	F_INP F_INN	I	1.25 GHz input - Positive and Negative (1000BASE-X and SGMII Media Interface 125 MHz Input - Positive and Negative (100BASE-FX) The fiber-optic transceiver's positive output connects to the F_INP. The fiber-optic transceiver's negative output connects to the F_INN.
60	SIGDET	I	SERDES signal detect 1 = Signal Detected 0 = No Signal Detected Polarity can be changed through register 16_1.9.
11 10	F_OUTP F_OUTN	O	1.25 GHz output - Positive and Negative (1000BASE-X and SGMII Media Interface 125 MHz output - Positive and Negative (100BASE-FX) The fiber-optic transceiver's positive input connects to the F_OUTP. The fiber-optic transceiver's negative input connects to the F_OUTN. Output amplitude can be adjusted via register 26_1.2:0.

Note

The fiber interface pins are not used for GBIC mode.

Table 3: MAC Interface

Pin #	Pin Name	Pin Type	Description
9 8	S_INP S_INN	I	SGMII Transmit Data. 1.25 GBaud input - Positive and Negative.
5 4	S_CLKP S_CLKN	O	SGMII 625 MHz Receive Clock output - Positive and Negative. Output amplitude can be adjusted via register 26_2.2:0
2 1	S_OUTP S_OUTN	O	SGMII Receive Data. 1.25 GBaud output - Positive and Negative. Output amplitude can be adjusted via register 26_2.2:0.
59	LOS	O	Loss of Signal/LED Status On hardware reset, LOS defaults to loss of signal where Hi-Z = Loss of Signal 0 = Media interface has link The LOS pin can be configured to output other status.

Note

The MAC interface pins are used for GBIC mode.

Table 4: Management Interface/Control

Pin #	Pin Name	Pin Type	Description
57	MDC/SSCL[1]	I	Management Clock pin. MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum frequency supported is 8.3 MHz. When the 88E1112 device is connected to a Two-Wire Serial Interface (TWSI) bus, MDC is connected to a serial clock line (SSCL). Data is stable during the high portion of the clock.
58	MDIO/SSDA[1]	I/O	Management Data pin. MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm When 88E1112 device is connected to a Two-Wire Serial Interface (TWSI) bus, MDIO connects to the serial data lines (SSDA). These pins are open-drain and maybe be wire-ORed with any number of open-drain devices. SSDA requires 1.5 kohm to 10 kohm pull-up resistors.

1. SSCL and SSDA pins should not be confused by the SCL and SDA pins. The SSCL, SSDA pins act like slaves in the TWSI bus. The SCL and SDA pins act like masters in EEPROM interface.

Table 5: EEPROM Interface

Pin #	Pin Name	Pin Type	Description
54	SCL	O	EEPROM Serial Clock
53	SDA	I/O	EEPROM Serial Data. This pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm

Table 6: Clock/Configuration/Reset/I/O Voltage Clamp Selection

Pin #	Pin Name	Pin Type	Description
48	CONFIG[0]	I	Configuration 0 pin
46	CONFIG[1]	I	Configuration 1 pin
45	CONFIG[2]	I	Configuration 2 pin
44	CONFIG[3]	I	Configuration 3 pin
42	CONFIG[4]	I	Configuration 4 pin
41	CONFIG[5]	I	Configuration 5 pin
38	STATUS[1]	O, mA	LED Status 1 pin
40	STATUS[0]	O, mA	LED Status 0 pin
61	INIT/INT	O	This is a triple function pin used for PHY Initialization, device interrupt, or LED Status. On hardware reset, INIT defaults to loss of signal where Hi-Z = PHY initialization is in process 0 = PHY registers initialized via EEPROM is complete The INIT pin can be configured to output other status.
36	XTAL1	I	25 MHz Clock Input 25 MHz ± 50 ppm tolerance crystal reference or oscillator input.
35	XTAL2	O	25 MHz Crystal Output. 25 MHz ± 50 ppm tolerance crystal reference. When the XTAL2 pin is not connected, it should be left floating.
52	RESET	I	Hardware reset. XTAL1 must be active for a minimum of 10 clock cycles before the rising edge of RESET. RESET must be in inactive state for normal operation. Reset Polarity is determined by POL_RST. See POL_RST below for details.
51	POL_RST	I, PU	Reset Polarity. If POL_RST = 1 or Unconnected 1 = Reset 0 = Normal operation If POL_RST = 0 1 = Normal operation 0 = Reset
50	PWRDN	I	1 = Power down 0 = Power up
49	NORMAL	I, PU	Test Mode Control 0 = Test mode 1 = Normal

Table 7: Test

Pin #	Pin Name	Pin Type	Description
25 26	HSDACP HSDACN	O	AC Test Point. Positive and Negative. These pins should be left floating but brought out for probing.
34	TSTPT	O	DC Test Point

Table 8: Reference

Pin #	Pin Name	Pin Type	Description
17	RSET	I	Resistor Reference External 5.0 kohm 1% resistor connected to ground.

Table 9: Power & Ground

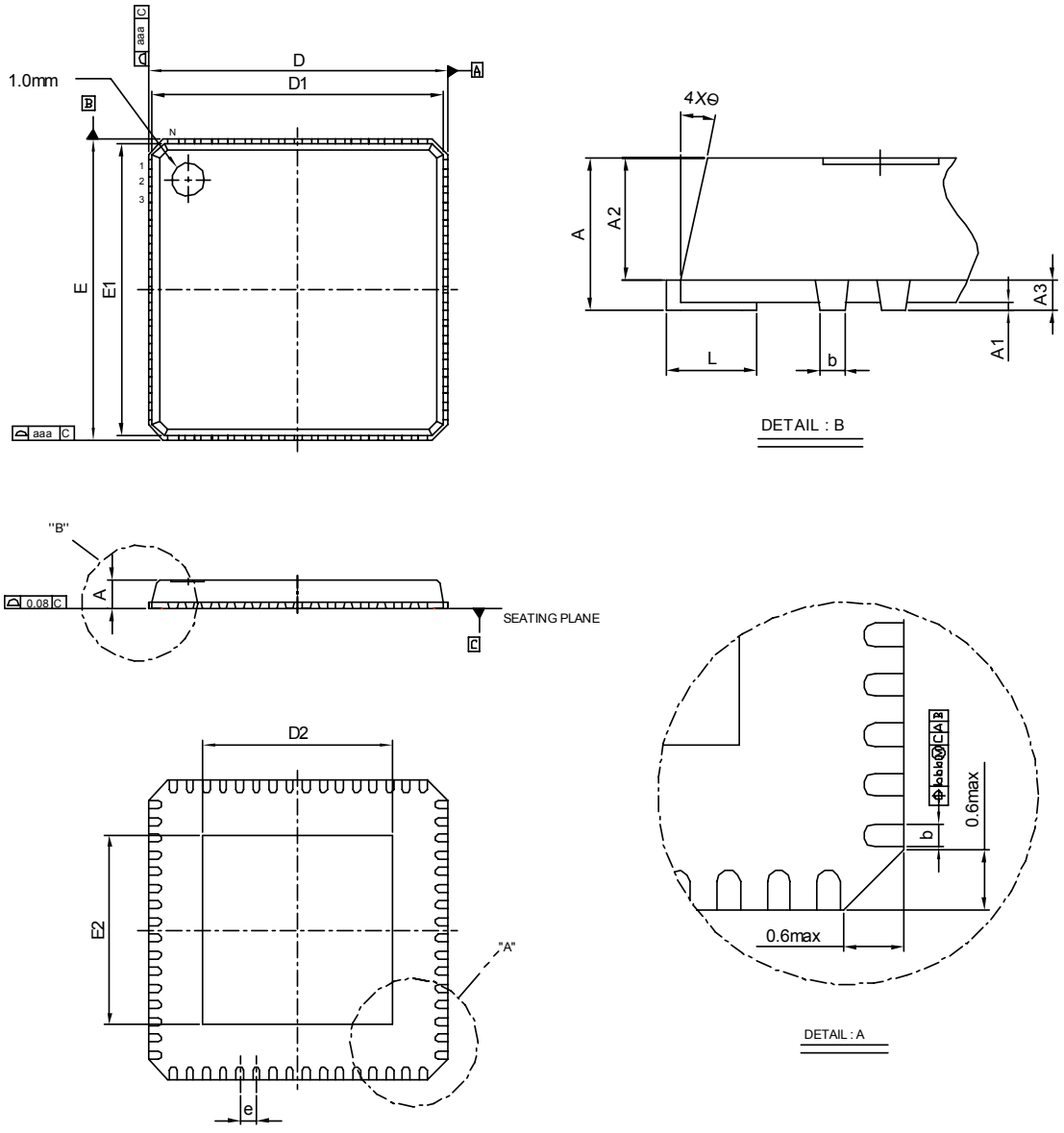
Pin #	Pin Name	Pin Type	Description
39 43 47 62 64	DVDD	Power	1.2V Digital Supply
12	F_VTT	Power	SERDES Output Supply
3	S_VTT	Power	SGMII Output Supply
20 23 24 29 33	VDDA	Power	2.5V Analog Supply.
37 56	VDDO	Power	1.5V or 2.5V I/O Supply. If the crystal option is used, VDDO must be connected to 2.5V. **NOTE:** I/O pins are not 3.3V tolerant when VDDO = 2.5V is used.
7 14	VDDAH	Power	2.5V Analog Supply.
6 13	VDDAL	Power	1.5V or 2.5V Analog Supply. 2.5V Analog Supply will draw more power.
EPAD 55 63	VSS	Ground	Ground. The 88E1112 device is contained in a 64 pin QFN package, which has an exposed die pad (E-PAD) at its base. The EPAD must be soldered to VSS. The location of the EPAD can be found in Section 2.1 "64 - Pin 9x9 mm QFN Package" on page 16 and Table 10, “64-Pin QFN Package Dimensions,” on page 17.
32	No Connect	NC	NC

1.3 64-Pin QFN Pin Assignment List - Alphabetical by Signal Name

Pin #	Pin Name	Pin #	Pin Name
48	CONFIG[0]	50	PWRDN
46	CONFIG[1]	52	RESET
45	CONFIG[2]	17	RSET
44	CONFIG[3]	54	SCL
42	CONFIG[4]	4	S_CLKN
41	CONFIG[5]	5	S_CLKP
39	DVDD	53	SDA
43	DVDD	60	SIGDET
47	DVDD	8	S_INN
62	DVDD	9	S_INP
64	DVDD	1	S_OUTN
15	F_INN	2	S_OUTP
16	F_INP	3	S_VTT
10	F_OUTN	40	STATUS[0]
11	F_OUTP	38	STATUS[1]
12	F_VTT	34	TSTPT
26	HSDACN	20	VDDA
25	HSDACP	23	VDDA
61	INIT/INT	24	VDDA
59	LOS	29	VDDA
57	MDC	33	VDDA
19	MDIN[0]	7	VDDAH
18	MDIP[0]	14	VDDAH
22	MDIN[1]	6	VDDAL
21	MDIP[1]	13	VDDAL
28	MDIN[2]	37	VDDO
27	MDIP[2]	56	VDDO
31	MDIN[3]	EPAD	VSS
30	MDIP[3]	55	VSS
58	MDIO	63	VSS
32	NC	36	XTAL1
49	NORMAL	35	XTAL2
51	POL_RST		

Section 2. Mechanical Drawings

2.1 64 - Pin 9x9 mm QFN Package



(All Dimensions in mm.)

Table 10: 64-Pin QFN Package Dimensions

Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.80	0.85	1.00
A1	0.00	0.02	0.05
A2	---	0.65	1.00
A3	0.20 REF		
b	0.18	0.23	0.30
D	9.00 BSC		
D1	8.75 BSC		
E	9.00 BSC		
E1	8.75 BSC		
e	0.50 BSC		
L	0.30	0.40	0.50
Θ	0°	---	12°
aaa	---	---	0.25
bbb	---	---	0.10
chamfer	---	---	0.60

Die Pad Size	
Symbol	Dimension in mm
D_2	5.21 ± 0.20
E_2	6.25 ± 0.20

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER

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