# Marvell® Alaska® C 88X9121P

Dual 400G, Quad 200G, Octal 100G Ethernet Transceiver with 100G Serial Electrical I/Os, 256 bit MACsec Encryption and Class C PTP Timestamping

## Overview

The Marvell Alaska C 88X9121P is a fully integrated single chip Ethernet transceiver with 100G serial I/Os that performs IEEE 802.1AE MACsec encryption with 256 bit key and IEEE 1588v2 PTP timestamping functionality for two ports of 400 GbE, four ports of 200 GbE or eight ports of 100 GbE. The device is targeted to drive next generation 400G/200G/100G optical modules in QSFPDD and OSFP form factors with 100G serial electrical I/Os. The X9121P supports 50G PAM4 and 25G/10G/1G NRZ signaling for 50GbE, 25GbE, 10GbE and 1GbE applications.

The device supports a variety of gearboxing modes to translate between 50G PAM4 and 100G PAM4 modes for 400GbE, 200GbE and 100GbE, with the necessary FEC termination and regeneration required to translate between the modes.

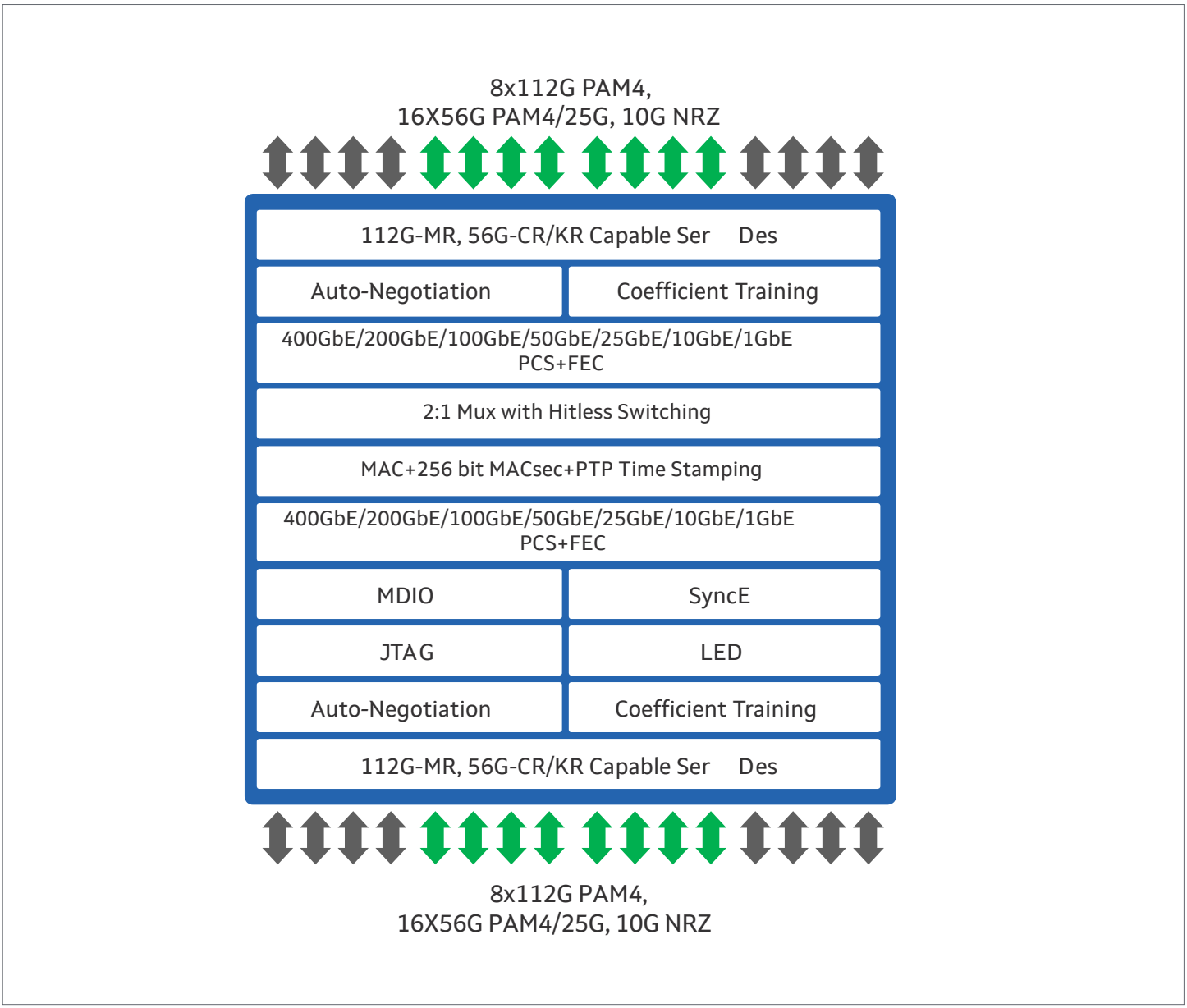
The PTP timestamping functionality in the device provides timing accuracy that meets the requirements of Class C profile, enabling high precision timing recovery required for wireless and carrier applications. The device provides recovered clock output for SyncE applications, with flexible clock source selection.

The 100G serial I/O on the X9121P is targeted to exceed the Chip to Module Interface specification for 100G serial electrical signaling being specified by IEEE 802.ck standard. For lower speeds, the Long Reach dual mode (PAM4 and NRZ) SerDes on the X9121P is fully compliant to the IEEE electrical specifications for transmission over passive direct attach cables and copper backplanes. The device supports FEC generation and termination capabilities for all FEC types defined by IEEE 802.3cd, 802.3by, 802.3bj, 802.3ba, 802.3ap and the 25 Gigabit Ethernet Consortium for 400GbE, 200 GbE, 100 GbE, 50 GbE, 40 GbE, 25 GbE, and 10 GbE operation. The supported FEC types include Clause-134 RS (544, 514), Clause-91 and Clause-108 RS (528, 514) RS-FEC, and FC (2212, 2080) FEC.

The device supports Auto-Negotiation and coefficient training protocol required by the IEEE 802.3 standards for operation over KR backplanes and CR passive copper cables. The device has a fully symmetric architecture with FEC generation and termination functionality, and AutoNegotiation and training capabilities on both host and line interfaces to provide complete system design flexibility.

The 88X9121P also supports 2:1 multiplexing functionality with hitless switching capability on the host interface to enable applications requiring redundancy.

**Block Diagram**




Marvell Alaska C 88X9121P Block Diagram

## Key Features

| Features | Benefits |
|---|---|
| Support for 100G Serial I/Os | · To drive next generation 400GbE, 200GbE and 100GbE optical modules with 100G serial electrical I/Os in QSFP-DD and OSFP form factors |
| Dual 400GbE, Quad 200GbE, Octal 100GbE, 16-port 50GbE, 25GbE, 10GbE, 1GbE MACsec with 256bit key | · Enables encrypted links for all speeds from 400GbE to 1GbE |
| Gearboxing between 50G PAM4 and 100G PAM4 modes for 400GbE, 200GbE and 100GbE | · Enables support of 1x100G PAM4 optics from switch ASICs with 50G PAM4 I/Os and vice versa |
| IEEE 1588v2 PTP Timestamping that meets timing accuracy requirements for Class C PTP profile | · Accurate extraction of timing information for timing-critical applications |
| Recovered clock for SyncE applications with flexible selection of clock | · Enables accurate transfer of clock over an Ethernet network |
| 2:1 Mux on the host interface with hitless switching | · For applications requiring Active/Standby redundancy with seamless switchover |
| Long Reach host and line interface SerDes | · For driving passive direct attach copper (DAC) cables and backplanes |
| Fully symmetric architecture with FEC capability on host and line interfaces | · Flexibility to support a wide range of applications and system design choices |
| Support for IEEE Auto Negotiation and Training protocol | · Seamless interoperability with standards-compliant devices from other vendors |
| 8x8 SerDes layer crossbar | · Enables board routing flexibility for the high speed I/Os |
| Ethernet packet and PRBS generation capabilities and eye monitoring capability on all high-speed interfaces | · Comprehensive debug capabilities |

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To deliver the data infrastructure technology that connects the world, we're building solutions on the most powerful foundation: our partnerships with our customers. Trusted by the world's leading technology companies for 25 years, we move, store, process and secure the world's data with semiconductor solutions designed for our customers' current needs and future ambitions. Through a process of deep collaboration and transparency, we're ultimately changing the way tomorrow's enterprise, cloud, automotive, and carrier architectures transform—for the better.



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